REMARKS

Claims 1-9 and 11-19 are pending in the case. All claims stand rejected. In the present submission, claims 1, 7, 8 and 12 have been amended and claims 6, 11 and 16 have been cancelled. Reconsideration is respectfully requested.

§101 Rejection

Claims 1-9 and 11-19 are rejected under 35 U.S.C. §101 because the claims are directed to non-statutory subject matter. Claims 6, 11 and 16 have been cancelled and the rejection as to these claims is now moot. In the present submission, independent claims 1 and 12 have been amended to recite the practical application accomplished by the claims. More specifically, claim 1 has been amended to recite "wherein the plurality of measurement parameters comprise temperature, voltage, bias current, and transmit power and receive power of an optical transceiver and the first parameter, being indicative of one of the measurement parameters, is selected to operate the device for supporting numerical value conversion of digital input values derived from multiple data sources." Claim 12 has been amended to recite "the plurality of measurement parameters comprising temperature, voltage, bias current, and transmit power and receive power of an optical transceiver" and "the first parameter being selected for supporting numerical value conversion of digital input values derived from multiple data sources."

As thus amended, Applicant submits that independent claims 1 and 12 and the dependent claims, 2-5, 7-9, 13-15 and 17-19 recite statutory subject matter. Withdrawal of the §101 is respectfully requested.

§103(a) Rejection

Claims 1-9 and 11-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelly (U.S. Patent 5,942,992) in view of Kawawaki et al. (5,371,694) and Ishida (U.S. Patent 5,504,697). Claims 6, 11 and 16 have been cancelled and the rejection as to these claims is now moot. Applicant respectfully traverses the rejection.

Claim 1, as amended, is patentable over the cited references at least by reciting "the N-bit digital input value comprises a digital input value with variable bit-lengths, the variable bit-lengths comprising a first bit length and a second bit length different than the first bit

length, the arithmetic logic unit generating a final digital output value being expressed in Q bits, the Q bits of the final digital output value comprising the digital output value of the arithmetic logic unit having the first bit length and trailing zeros or the digital output value having the second bit length and trailing zeros."

The claimed invention of claim 1 is capable of supporting digital input values having variable bit-length and is further capable of providing digital output values having various resolution. The ***final*** digital output value is expressed in Q bits where trailing zeros are added to the digital output value of the arithmetic logic unit having different bit length. Some of the amendments made in claim 1 were previously presented in claim 11 and all of the amendments to claim 1 are supported by Applicant's specification, paragraphs [0047] to [0053].

Neither Kelly, nor Kawawaki, nor Ishida teach or suggest supporting digital input values having different bit lengths. More importantly, none of the cited references teach or suggest providing digital output values having different resolution but expressed in Q bits by using trailing zeros. Claim 1 is therefore patentable over the cited references. Claims 2-5 and 7-9, dependent upon claim 1, are therefore also patentable for at least the same reasons claim 1 is patentable.

Claim 12, as amended, is patentable over the cited references at least by reciting "the N-bit digital input value comprises a digital input value with variable bit-lengths, the variable bit-lengths comprising a first bit length and a second bit length different than the first bit length, the arithmetic logic unit generating a final digital output value being expressed in Q bits, the Q bits of the final digital output value comprising the digital output value of the arithmetic logic unit having the first bit length and trailing zeros or the digital output value having the second bit length and trailing zeros." For the same reasons discussed above with reference to claim 1, claim 12 is patentable over the cited references. Claims 13-15 and 17-19, dependent upon claim 12, are therefore also patentable for at least the same reasons claim 12 is patentable.

CONCLUSION

After the present amendment, claims 1-5, 7-9, 12-15 and 17-19 are pending in the present application. For the reasons stated above, the application is in condition for allowance and passage of the present case to allowance is respectfully requested. If the Examiner would like to discuss any aspect of this application, the Examiner is invited to contact the undersigned at (408) 382-0480.

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/Carmen C Cook/	October 15, 2007
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Respectfully submitted,

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